REMARKS

Prior to the present response, claims 1-3, 6-8, 11-15, and 18-20 were pending in the present application, and now remain in the application. Claims 1-3 and 6-8 have been allowed. Reconsideration and allowance of outstanding claims 11-15 and 18-20 in view of the following remarks are requested.

A. Applicant Respectfully Requests the Withdrawal of the Finality of the Present First Action

Applicant notes that among conditions for making a first action a final action are that the new application be "a *continuing application* of, or a substitute for, an earlier application," AND that "*all claims of the new application (1) are drawn to the same invention claimed in the earlier application* and (2) . . . ." MPEP §706.07(b) (2005) (emphases added). Applicant respectfully submits that neither of these two conditions is satisfied in the present case. As such, the primary examiner is requested to withdraw the finality of the present first action, as required under MPEP §706.07(c) (2005).

First, a Request for Continued Examination is not a "continuation application." The applicable rules and the MPEP make this distinction clear. For example, the MPEP states that "35 U.S.C. 132(b) provides for continued examination of an application at the request of the applicant (request for continued examination or RCE) upon payment of a fee, *without requiring the applicant to file a continuing application* under 37 CFR 1.53(b)." MPEP §706.07(h) (2005) (emphasis added). In fact, a continuing application is

treated as a new application and is assigned a new Serial Number. In contrast, an RCE is not a new application; but merely a request to continue prosecution of the same application - and no new Serial Number is assigned.

Second, for the first action to be a final action, all claims of the new application are required to be drawn to the same invention claimed in the earlier application. That is not the case here. Even if the present RCE was treated as a continuing application, all independent claims were amended concurrently with the RCE filing. The amended claims are, by definition, drawn to a different invention. Even if the Examiner believes that the difference is small (and Applicant believes that the difference is not small), it is not deniable that an amended claims is not the same as a previously presented claim. Stated differently, Applicant enjoys a statutory right to file an RCE so that the amendments can be substantively considered in a non-final office action and, if the amendments are deemed insufficient by the Examiner, Applicant would have an opportunity to make additional arguments to the Examiner in response to a subsequent final office action. Thus, Applicant submits that it is improper to make the first office action a final action in the circumstances of the present RCE filing.

B. <u>Rejections of Claims 11-15 and 18-20 under 35 USC §102(e)</u>

The Examiner has rejected claims 11-15 and 18-20 under 35 USC §102(e) as being anticipated by U.S. Patent Application Publication Number US 2001/0042190 to Tremblay, et al. ("Tremblay"). For the reasons discussed below, Applicant respectfully

submits that the present invention, as defined by independent claims 11 and 19, is patentably distinguishable over Tremblay.

As disclosed in the present application, conventional approaches in the field of processor architectures do not adequately resolve the problem of excessive consumption of the chip area by wide buses, such as wide "move" buses linking various register file banks. Various embodiments according to the present invention address and overcome the need in the art for reducing the chip area and also speeding up the processor and reducing power consumption in a very long instruction word ("VLIW") processor, while accommodating multiple register file banks and multiple execution units.

An exemplary embodiment of the present invention, as shown in Figure 2, includes register file banks 252 and 254. Register file bank 252 comprises read ports 280 and write ports 282, while register file bank 254 comprises read ports 290 and write ports 292. Data path block 212 comprises execution units such as multipliers 216 and 220 and ALUs ("arithmetic logic unit") 218 and 222, while data path block 214 comprises execution units such as multipliers 224 and 230 and ALUs 226 and 228.

Furthermore, read buses 260 and 262 connect register file bank 254 to data path block 212 and read buses 264 and 266 connect register file bank 252 to data path block 214. Accordingly, operands present in register file bank 254 are accessed by data path block 212 through read buses 260 and 262 while operands existing in register file bank 252 are concurrently accessed by data path block 214 through read buses 264 and 266.

Moreover, a result of an operation performed in data path block 212 is only written to write ports 282 in register file bank 252, whereas a result of an operation performed in data path block 214 is only written to write ports 290 in register file bank 254.

In addition, as seen in Figure 3, scheduling restrictions are imposed on the relationship between read ports, buses, and execution units included in the present invention. For example, during a single clock cycle, read bus 264 is utilized to transport an operand from read port R0 in register file bank 252 to either multiplier 224 or ALU 226 in data path block 214. See, for example, present application, page 17, lines 16-18. Consequently, the present invention avoids the need for a wider bus that can accommodate concurrent transport of two operands, one to multiplier 224 and another to ALU 226. Therefore, the scheduling restrictions result in area savings since the need for additional ports and wider buses is avoided. Furthermore, since the read buses are narrower and efficiently used during execution of instructions, excess power consumption is eliminated and significant power savings also result.

In contrast, Tremblay discloses a VLIW processor having a plurality of functional units, for example, as seen in Figure 2, media functional unit (MFU) 220 and general functional unit (GFU) 222. GFU 222, for example, "is a RISC processor capable of executing arithmetic logic unit (ALU) operations, loads and stores, branches, and various specialized and esoteric functions..." Tremblay, paragraph 36, lines 1-4. Tremblay further discloses that "media functional units 220 are multiple single-instruction-multiple-datapath (MSIMD) media functional units." Tremblay, paragraph 35, lines 11-13. Since

the functional units in Tremblay (e.g., MFU 220 and GFU 222) each include multiple execution units (e.g., ALU, load, and store features of GFU 222 and multiple data path features of MFU 220), the functional units in Tremblay are not comparable to the execution units in the present invention.

As previously discussed, each data path block in the present invention (e.g., data path block 212) comprises execution units (e.g., multiplier 216, ALU 218, multiplier 220). The scheduling restrictions disclosed and claimed in the present invention apply to the execution units included in each data path. Thus, since the functional units in Tremblay are not comparable to the execution units in the present invention, Tremblay does not teach, disclose, or suggest any such scheduling restrictions with respect to any execution units. As such, Tremblay does not teach, disclose or suggest a VLIW processor "wherein during a single clock cycle an operand residing in one of said first plurality of read ports is used by only one of said first plurality of *execution units* in said first data path block..." as required by independent claim 11, or a VLIW processor "wherein during a single clock cycle an operand residing in one of said respective plurality of read ports is used by only one of said respective plurality of *execution units*..." as required by independent claim 19.

In contrast to the disclosure in Tremblay, the disclosed and claimed scheduling restrictions in the present invention result in area savings since the need for additional ports and wider buses are avoided. See, for example, present application, page 19, lines 12-13. Moreover, since the read buses are narrower and fully utilized during execution of

instructions, excess power consumption is eliminated and significant power savings also result. See, for example, present application, page 19, lines 14-16. The Examiner, however, states that "'a wider bus' and 'providing the area and power savings are not the claimed subject matter.'" Present office action, page 8. The above-mentioned advantages provided by the present invention, as disclosed in the detailed description, are the natural results of the disclosed and claimed invention and have been set forth to illustrate the shortcomings of the configuration disclosed in Tremblay.

For the foregoing reasons, Applicant respectfully submits that the present invention as defined by independent claims 11 and 19, is not taught, disclosed, or suggested by the art of record. As such, the claims depending from independent claims 11 and 19 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim.

C. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 11 and 19, and the claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, outstanding claims 11-15 and 18-20 are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance directed to all claims 1-3, 6-8, 11-15, and 18-20 remaining in the present application is respectfully requested.

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Respectfully Submitted,
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